AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph at page 2, line 15 as follows:

Figure[[s]] 1 shows a basic block diagram; and

Please amend the paragraph at page 3, lines 3-5 as follows:

Current frame times are preferably either approximately 33 milliseconds for a 30-frames per second system, or approximately 16 milliseconds for high motion resolution of 60 ~~miliseconds.~~ frames per second.

Please amend the paragraph at page 3, lines 11-13 as follows:

The signal integration process is divided into two parts: an analog part in the active pixel sensor 100 and a digital part in digital random access memory[[.]] 110.

Please amend the paragraph at page 3, lines 14-22 as follows:

A first embodiment is shown in FIG. 2. ~~Fig.~~ FIG. 2 shows the active pixel sensor array 100, coupled with an analog signal processor 202, column A/D converters 204, ~~and~~ a digital processor 206,[[.]] and a digital memory array 110a of the digital memory 110. The analog signal processor 202 includes column analog double sampling circuitry for sampling both signals and references to decrease the pixel fixed pattern noise.

Preamplifiers with adjustable gains, can also be used to increase the sensitivity and provide an automatic exposure control, as is known in the art.

Please amend the paragraph at page 4, lines 8-14 as follows:

The digital signal processor (DSP) 206 provides arithmetic operations such as addition, subtraction, division, and multiplication, and also includes a buffer memory to maintain intermediate results. DSP 206 can also act to digitally correct column digital fixed pattern noise. FIG. 3 shows a system similar to that in FIG. 2 but with twice as many digital memory arrays 110a and processing circuits[[.]] 206.

Please amend the paragraph at page 4, lines 15-21 as follows:

In operation, the sensor is preferably a CMOS image sensor that is of a sufficiently small size that it cannot integrate for a desired frame period. The information from the sensor is sampled by the column A/D converts 204 at an oversampled rate. Each sample is stored in the digital memory array[[,]] 110a, and the values are integrated in that memory[[.]] 110a. A digitally integrated value can be subsequently read from the digital memory array[[.]] 110a.